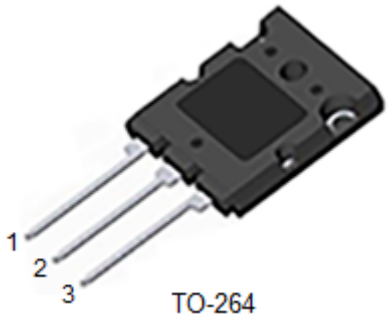
1. Features

- Advanced Planar Process
- $R_{DS(ON)}$=280mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

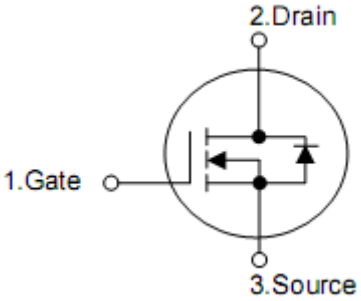
2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Pin configuration



TO-264



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNK7880A	TO-264	KIA

5. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}	800	V
Gate-to-Source Voltage	V_{GSS}	±30	
Continuous Drain Current	I_D	27	A
Continuous Drain Current @ Tc=100 ºC		17	A
Pulsed Drain Current at V_{GS}=10V [2),4)]	I_{DM}	108	A
Single Pulse Avalanche Energy	EAS	4200	mJ
Peak Diode Recovery dv/dt [3)]	dv/dt	5	V/ns
Power Dissipation	P_D	650	W
Derating Factor above 25 ºC		5.2	W/ºC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300 260	ºC
Storage Temperature Range	T_J& T_{STG}	-55 to 150	ºC

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.192	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	55	ºC/W

7. Electrical characteristics

(T_J=25°C,unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	800	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0V	-	-	5	uA
		V_{DS}=640V, VGS=0V, T_J=125°C	-	-	125	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-to-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=13.5A	-	280	350	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.5	-	4.5	V
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=12A	-	18	-	S
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, f=1.0MHZ	-	7280	-	pF
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Output Capacitance	C_{oss}		-	660	-	
Total Gate Charge	Q_g	V_{DD}=400V,I_D=13A, V_{GS}=0~10V	-	185	-	nC
Gate-to-Source Charge	Q_{gs}		-	42	-	
Gate-to-Drain (Miller) Charge	Q_{gd}		-	62	-	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD}=400V, I_D=13A, R_G=10Ω,V_{GS}=10V	-	56	-	nS
Rise Time	t_{rise}		-	105	-	
Turn-Off Delay Time	$t_{d(OFF)}$		-	82	-	
Fall Time	t_{fall}		-	96	-	
Continuous Source Current[2)]	I_{SD}	Integral PN-diode in MOSFET	-	-	27	A
Pulsed Source Current[2)]	I_{SM}		-	-	108	A
Forward Voltage	V_{SD}	I_S=27A, V_{GS}=0V	-	-	1.5	V
Reverse recovery time	t_{rr}	V_{GS}=0V ,I_F=27A, diF/dt=-100A/μs	-	900	-	ns
Reverse recovery charge	Q_{rr}		-	2.0	-	uC

Note:
1) T_J=+25 to +150
2) Silicon limited current only.
3) Package limited current.
4) Repetitive rating; pulse width limited by maximum junction temperature.
5) Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

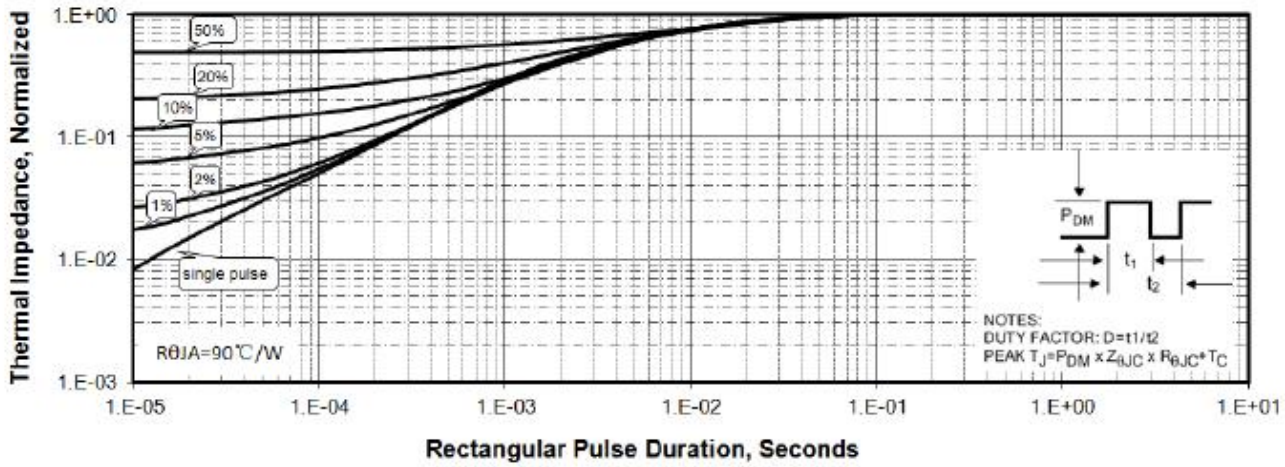


Figure 2 . Max. Power Dissipation vs Case Temperature

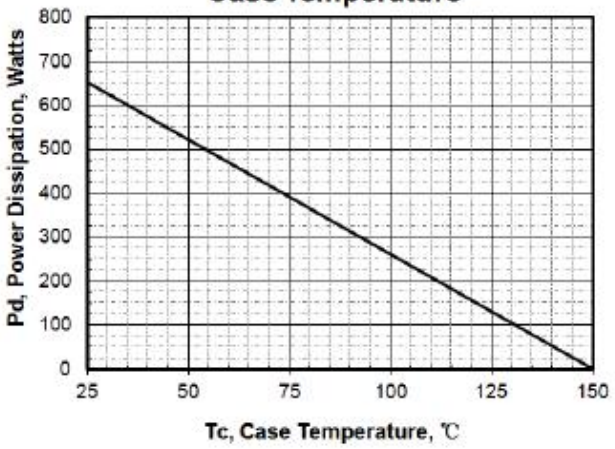


Figure 3 .Maximum Continuous Drain Current vs Tc

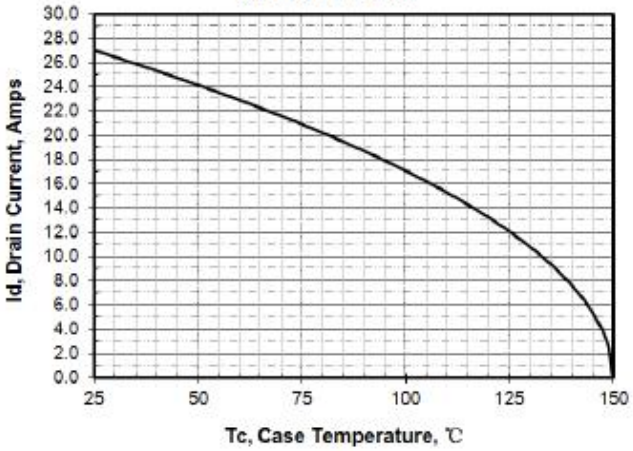


Figure 4. Output Characteristics

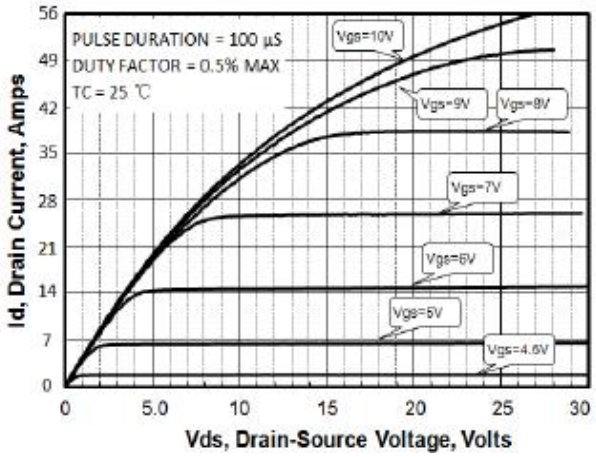


Figure 5. Rdson vs Gate Voltage

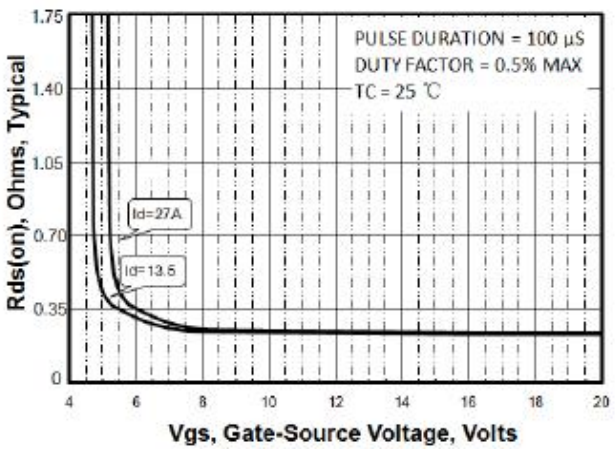


Figure 6. Peak Current Capability

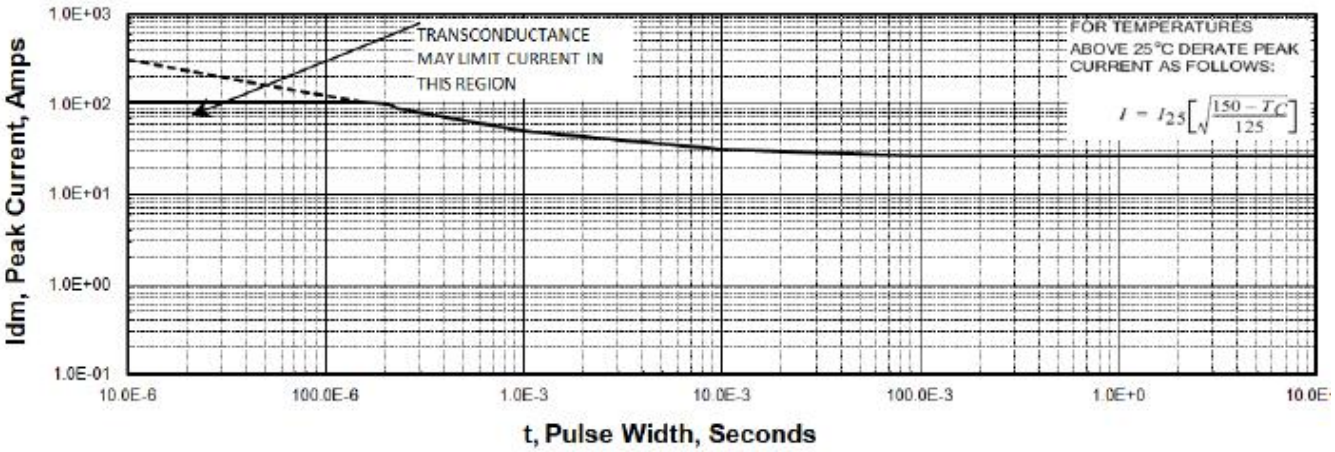


Figure 7. Transfer Characteristics

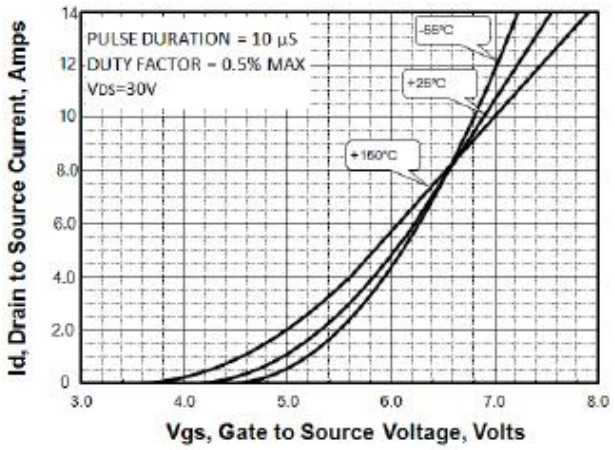


Figure 8. Unclamped Inductive Switching Capability

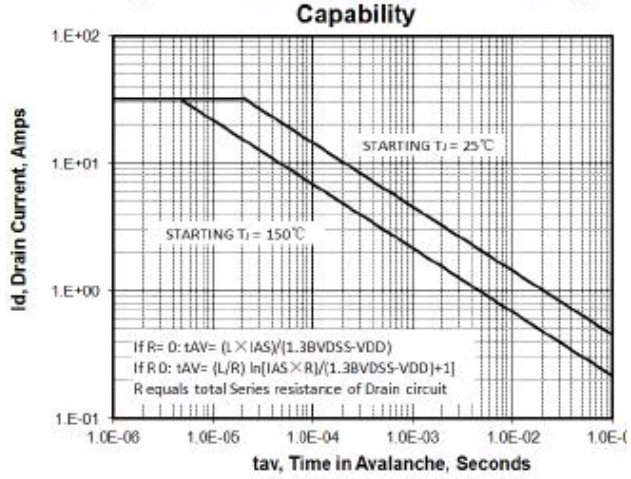


Figure 9. Drain to Source ON Resistance vs Drain Current

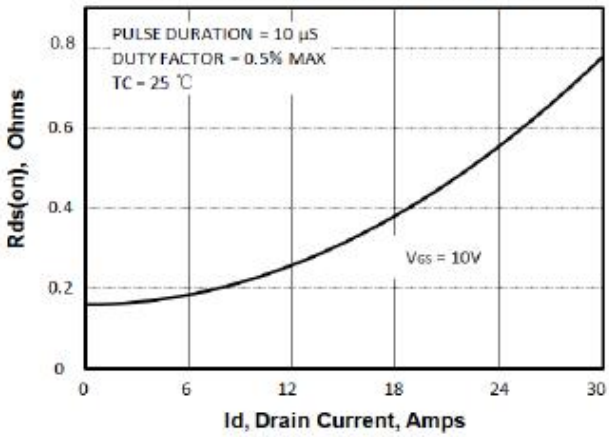


Figure 10. Rdson vs Junction Temperature

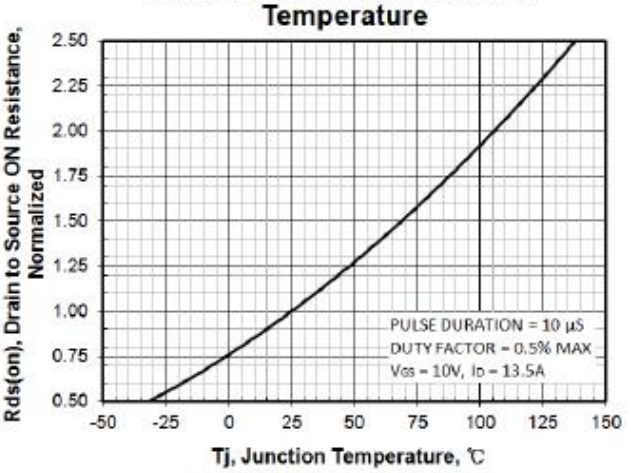


Figure 11.Breakdown Voltage vs Temperature

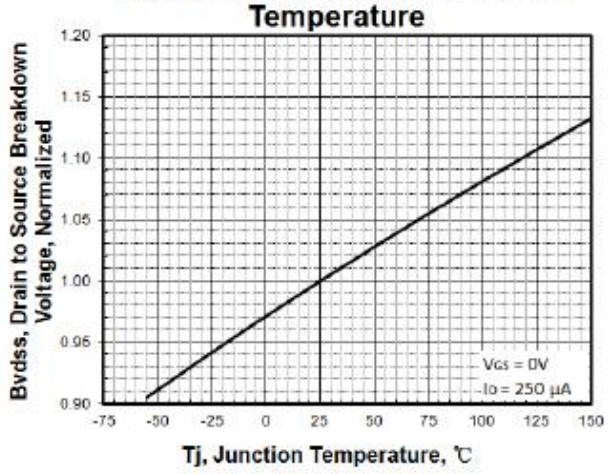


Figure 12.Threshold Voltage vs Temperature

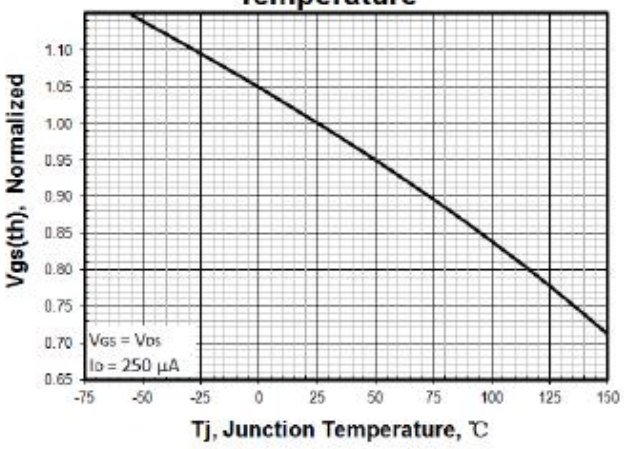


Figure 13 . Maximum Safe Operating Area(TO-247)

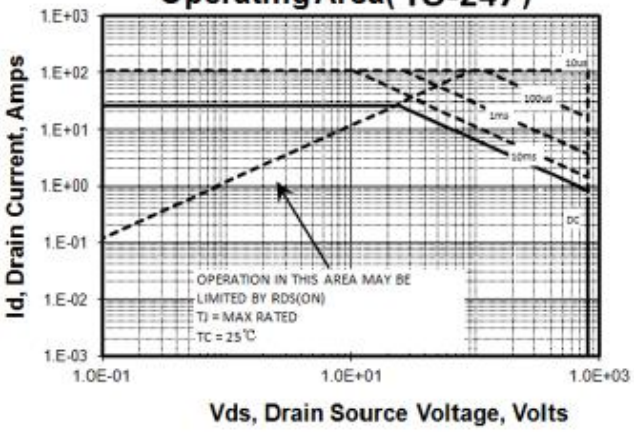


Figure 14. Capacitance vs Vds

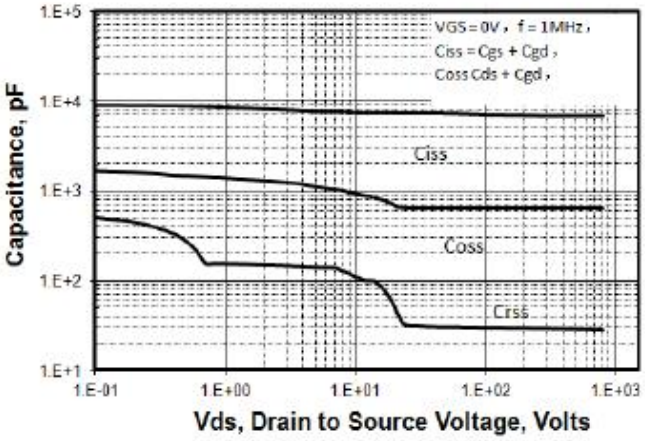


Figure 15 .Typical Gate Charge

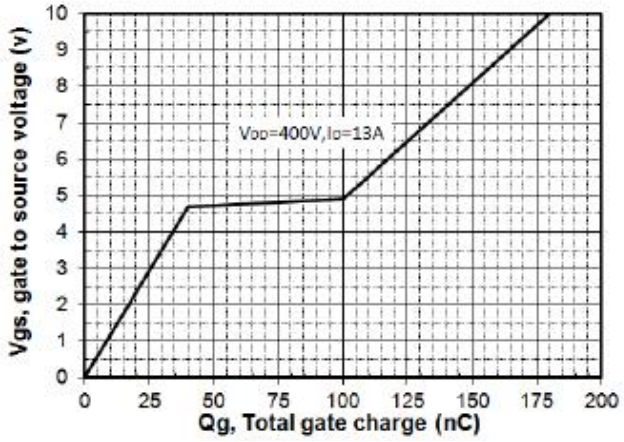
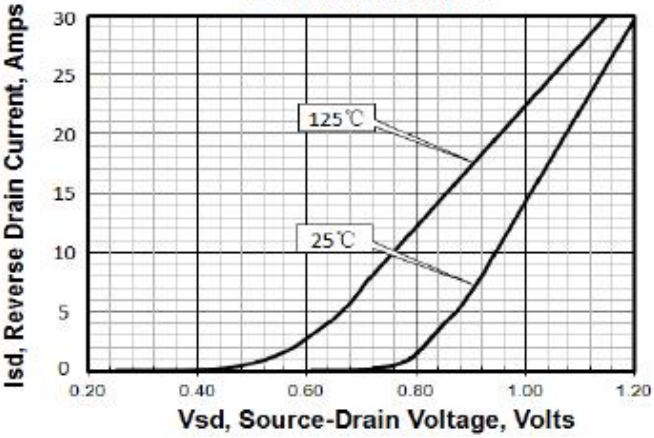


Figure 16.Body Diode Transfer Characteristics



9.Test Circuits and Waveforms

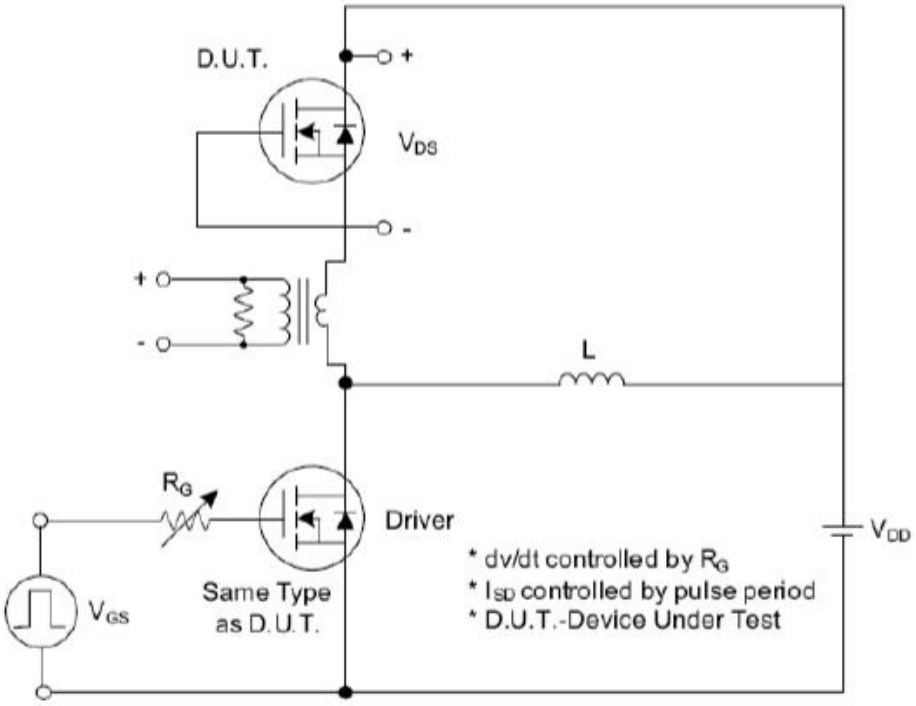


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

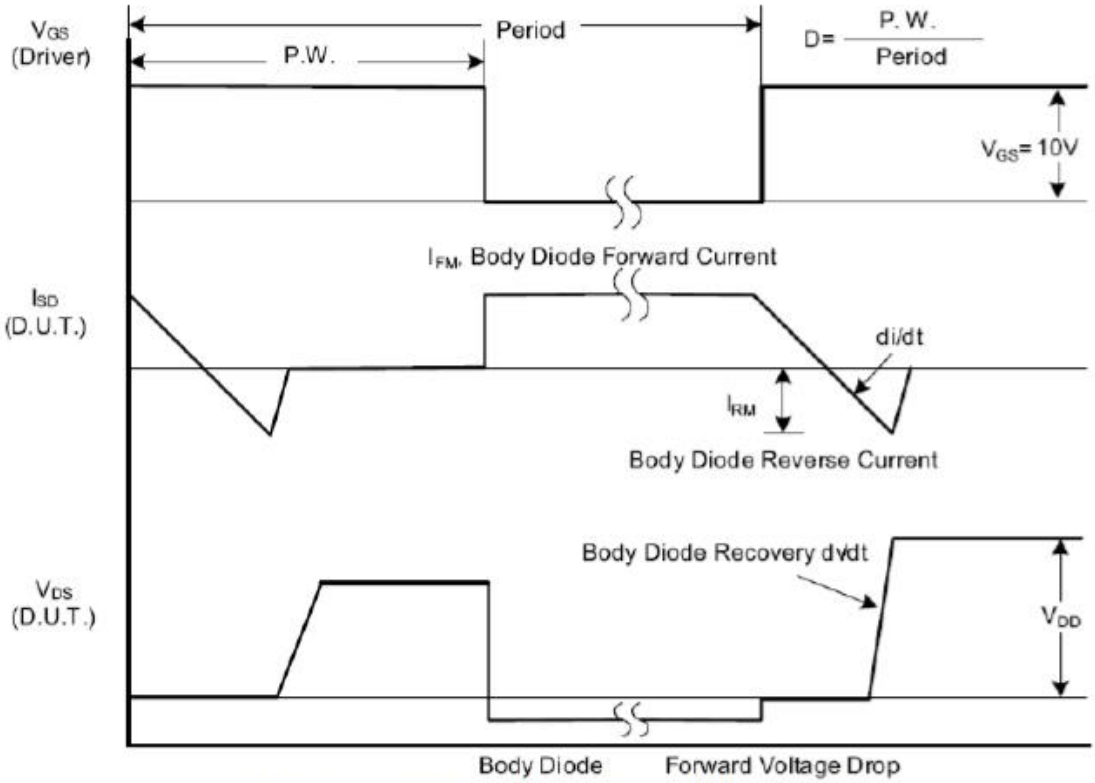


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

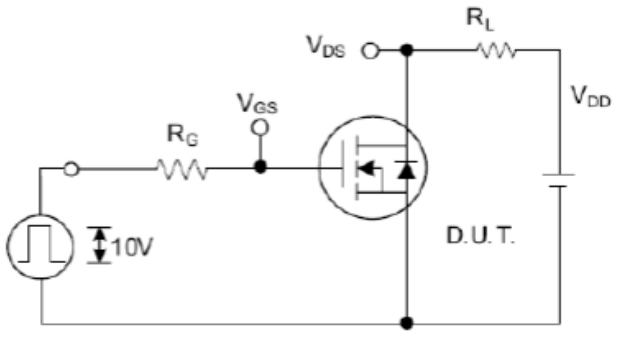


Fig. 2.1 Switching Test Circuit

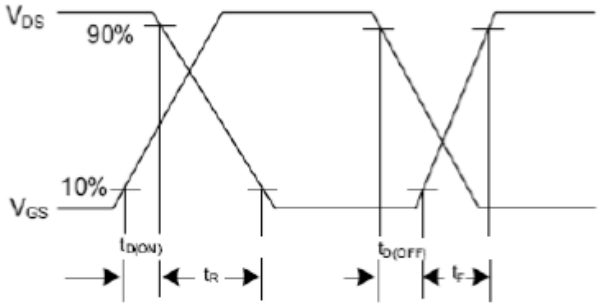


Fig. 2.2 Switching Waveforms

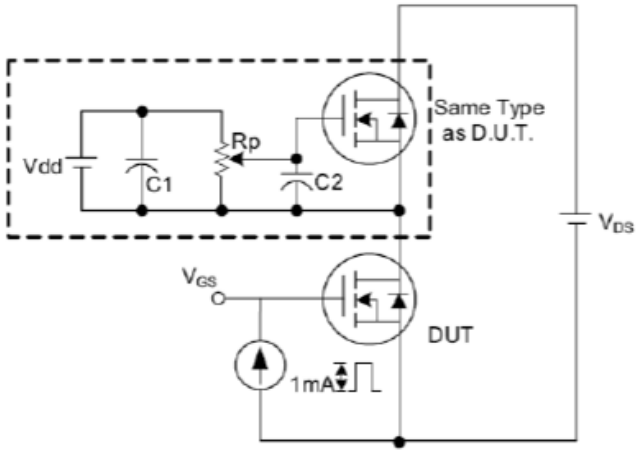


Fig. 3 . 1 Gate Charge Test Circuit

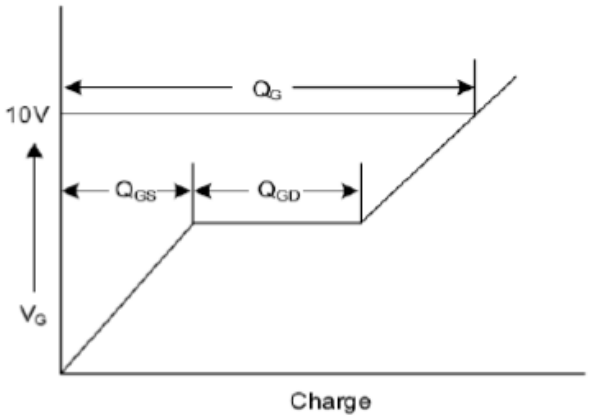


Fig. 3 . 2 Gate Charge Waveform

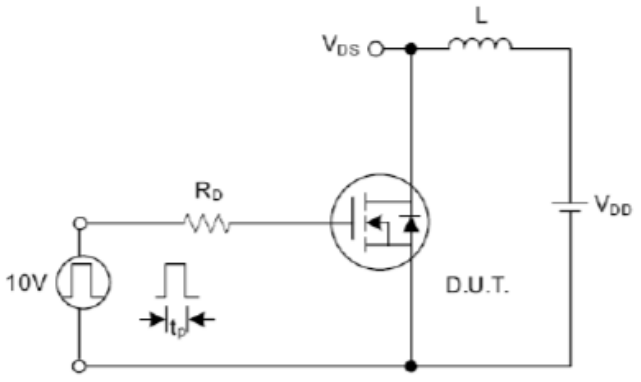


Fig. 4.1 Unclamped Inductive Switching Test Circuit

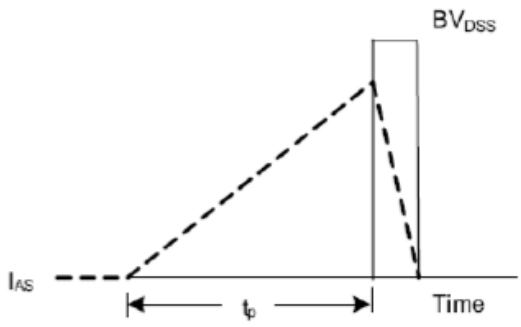


Fig. 4.2 Unclamped Inductive Switching Waveforms