

1. Description

The KIA-8103A is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA30N03B meet the RoHS and Green Product requirement, 100%EAS guaranteed with full function reliability approved.

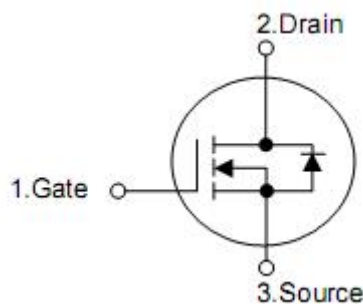
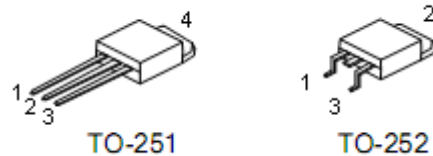
2. Features

- n $R_{DS(on)}=15m\Omega @ V_{DS}=30V$
- n Advanced high cell density Trench technology
- n Super Low Gate Charge
- n Excellent Cdv/dt effect decline
- n 100%EAS Guaranteed
- n Green Device Available

3. Applications

- n High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- n Networking DC-DC Power System
- n Load Switch

4. Symbol



Pin	Function
1	Gate
2	Drain
3	Source

5. Ordering Information

Part Number	Package	Brand
KND9120A	TO-252	KNX
KNU9120A	TO-251	KNX

6. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20	V
Continuous drain current, $V_{GS} @ 10V^1$	I_D	$T_C=25^{\circ}C$	A
		$T_C=100^{\circ}C$	A
Pulsed drain current ²	I_{DM}	60	A
Single pulse avalanche energy ³	E_{AS}	72	mJ
Avalanche current	I_{AS}	21	A
Total power dissipation ⁴	P_D	25	W
Operation junction temperature range	T_J	-55 to 150	$^{\circ}C$
Storage temperature range	T_{STG}	-55 to 150	$^{\circ}C$

7. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance, Junction-ambient ($t \leq 10s$) ¹	$R_{\theta JA}$	--	25	$^{\circ}C/W$
Thermal resistance, Junction-ambient (Steady State) ¹	$R_{\theta JA}$	--	62	$^{\circ}C/W$
Thermal resistance, Junction-case ¹	$R_{\theta JC}$	--	5	$^{\circ}C/W$

8. Electrical characteristics

(T_J=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
BV _{DSS} temperature coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25 °C, I _D =1mA		0.023		V/°C
Static drain-source on-resistance ²	R _{DS(on)}	V _{GS} =10V, I _D =10A		15	18	mΩ
		V _{GS} =4.5V, I _D =5A		22	30	
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.5	V
V _{GS(th)} temperature coefficient	ΔV _{GS(th)}			-5.2		mV/°C
Drain-source leakage current	I _{DSS}	V _{DS} =24V, V _{GS} =0V T _J =25°C			1	μA
		V _{DS} =24V, V _{GS} =0V T _J =55°C			5	μA
Gate- source leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Forward transconductance	g _{fs}	V _{DS} =15V, I _D =10A		10		S
Gate resistance	R _g	V _{DS} =24V, V _{GS} =0V, f=1MHz		2.5	5	Ω
Total gate charge(4.5V)	Q _g	V _{DS} =20V, V _{GS} =4.5V I _D =12A	-	7.2		nC
Gate-source charge	Q _{gs}			1.4		
Gate-drain charge	Q _{gd}			2.2		
Turn-on delay time	t _{d(on)}	V _{DD} =12V, I _D =5A, R _G =3.3Ω, V _{GS} =10V		4.1		ns
Rise time	t _r			9.8		
Turn-off delay time	t _{d(off)}			15.5		
Fall time	t _f			6.0		
Input capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz		572		pF
Output capacitance	C _{oss}			81		
Reverse transfer capacitance	C _{rss}			65		
Single pulse avalanche energy ⁵	EAS	V _{DD} =25V, L=0.1mH, I _{AS} =10A	16			mJ
Continuous source current ^{1,6}	I _S	V _G = V _D =0V, Force current			30	A
Pulsed source current ^{2,6}	I _{SM}				60	A
Diode forward voltage ²	V _{SD}	V _{GS} =0V, I _S =15A, T _J =25°C			1.2	V

Note:1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2.The data tested by pulsed, pulse width≤300μs, duty cycle≤2%

3.The EAS data shows Max.rating.The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A

4.The power dissipation is limited by 150°C junction temperature

5.The Min, value is 100% EAS tested guarantee.

6.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

9. Test circuits and waveforms

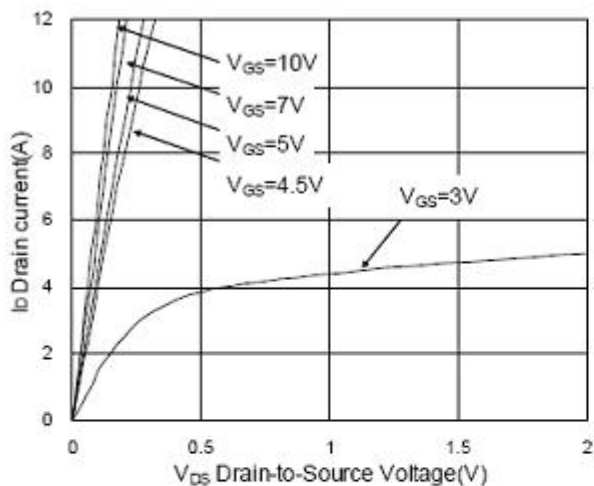


Fig.1 Typical Output Characteristics

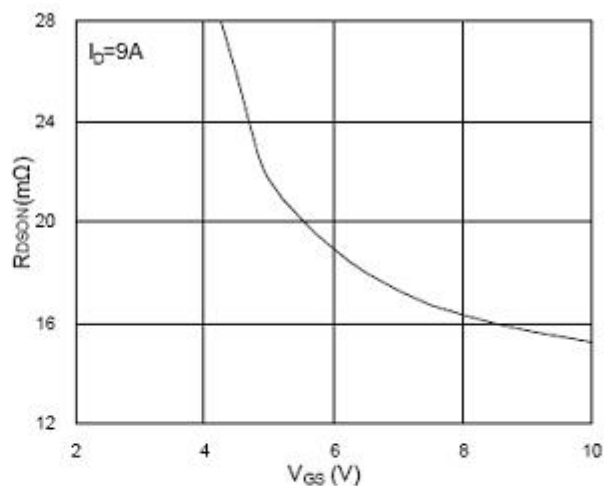


Fig.2 On-Resistance v.s Gate-Source.

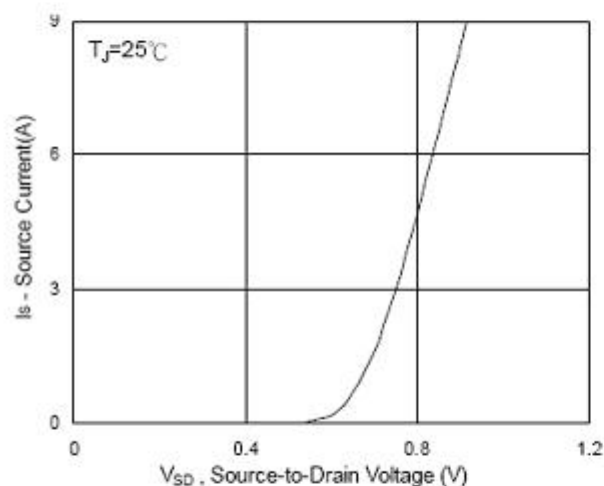


Fig.3 Forward Characteristics of Reverse

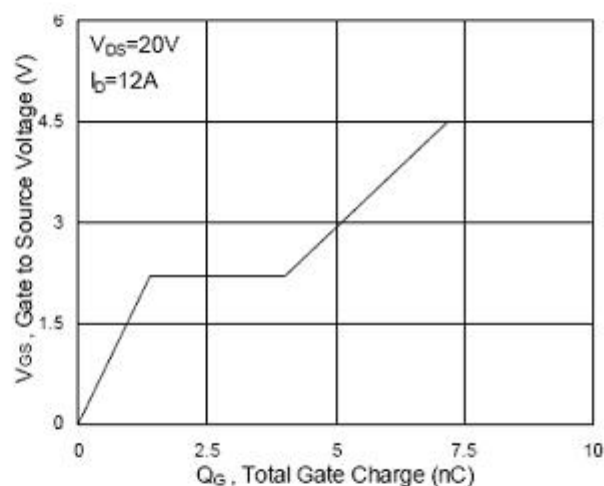


Fig.4 Gate-Charge characteristics

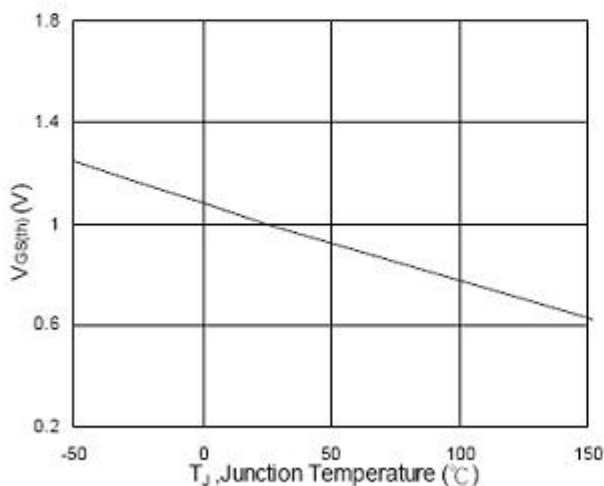


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

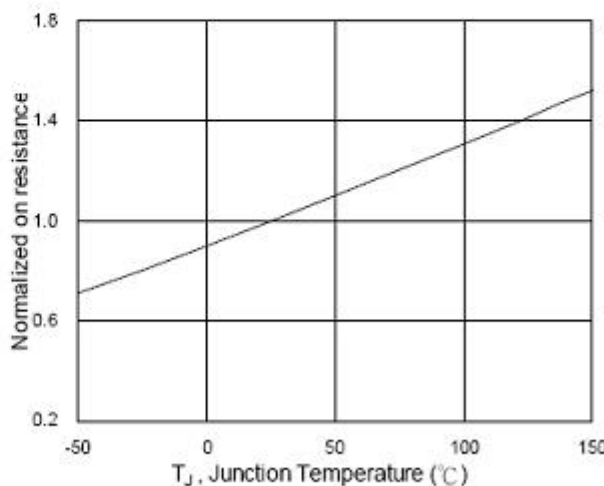


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

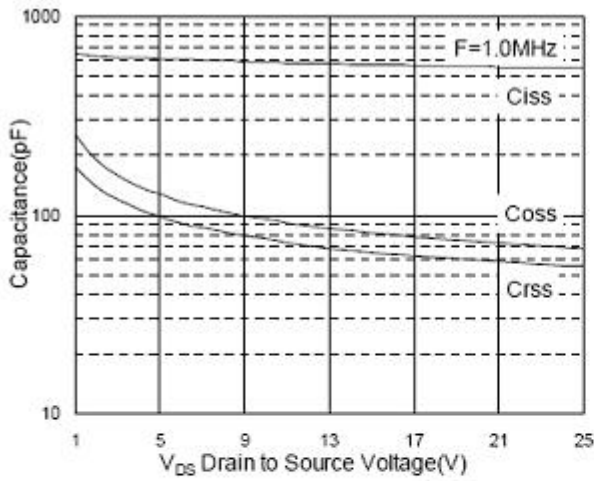


Fig.7 Capacitance

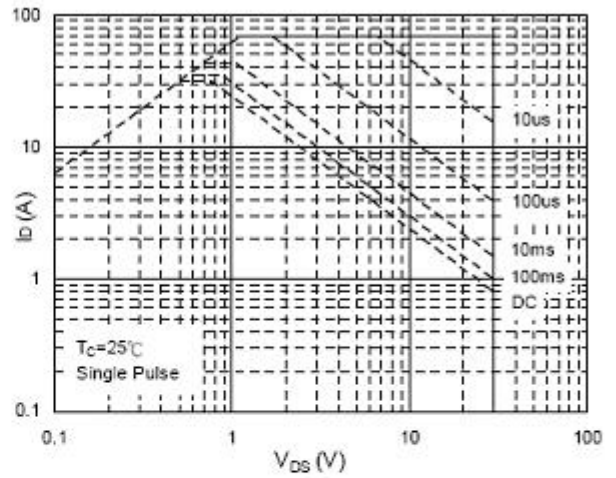


Fig.8 Safe Operating Area

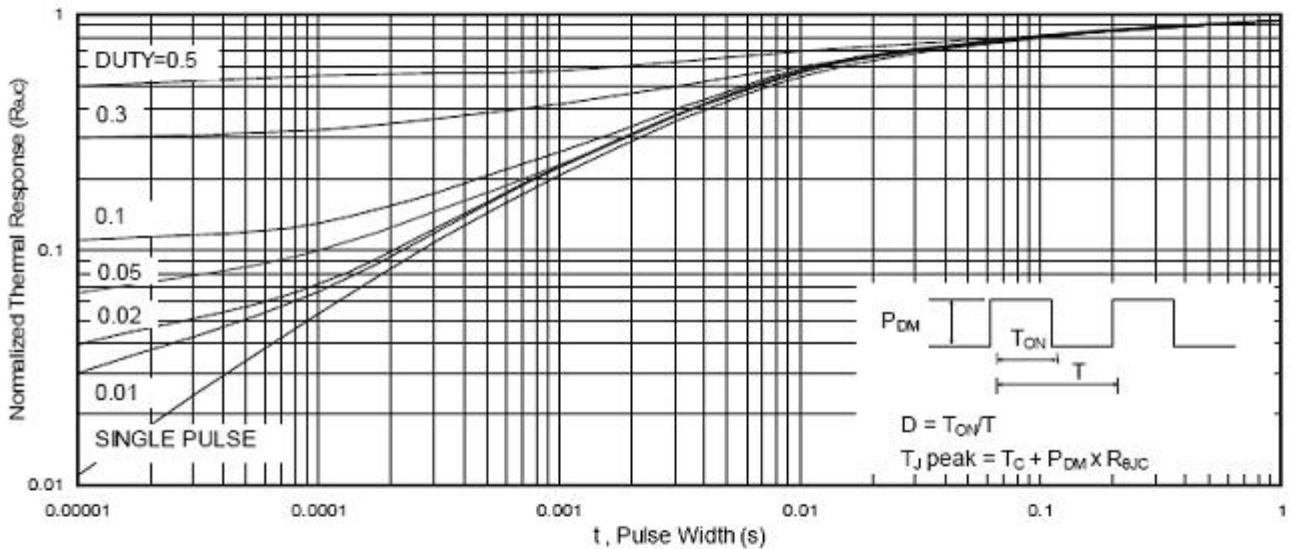


Fig.9 Normalized Maximum Transient Thermal Impedance

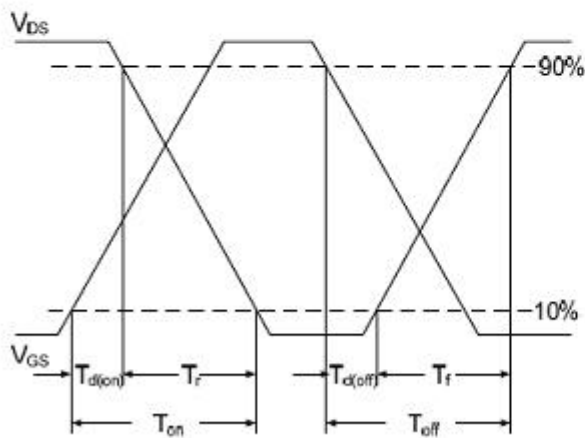


Fig.10 Switching Time Waveform

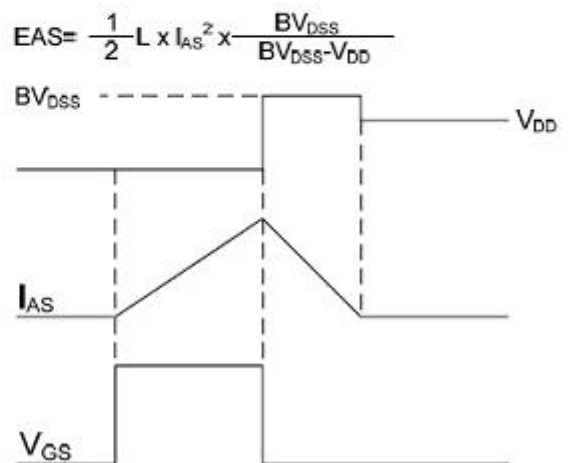


Fig.11 Unclamped Inductive Switching Waveform