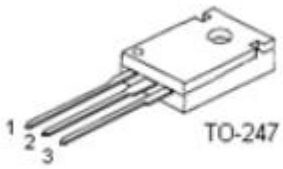
1. Applications

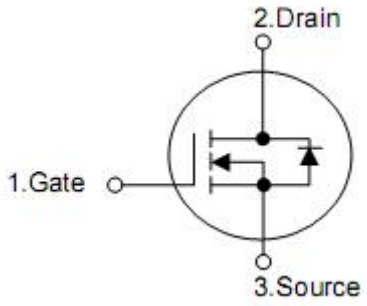
- DC-DC converters and Off-line UPS
- High efficiency synchronous rectification in SMPS

2. Features

- $R_{DS(on)}$=5.0mΩ @V_{GS}= 10 V
- Super high dense cell design
- Ultra low On-Resistance
- 100% avalanche tested
- Lead Free and Green devices avallable (RoHS Compliant)

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source

4. Absolute maximum ratings

(T_C=25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings	Units
Drain-source voltage		V_{DSS}	75	V
Gate-source voltage		V_{GSS}	±25	V
Continuous drain currenet T_C=25 ºC[1]		I_D	150	A
Continuous drain currenet T_C=100 ºC[1]			111	A
300us pulsed drain current tested T_C=25 ºC[2]		I_{DP}	600	A
Avalanche energy single pulse[3]		E_{AS}	784	mJ
Power dissipation	T_C=25 ºC	P_D	350	W
	T_C=100 ºC		175	W
Maximum junction temperature		T_J	175	℃
Storage temperature range		T_{STG}	-55~+175	℃
Diode continuous forward current T_C=25 ºC[1]		I_S	150	A

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-to-case	θ_{JC}	0.5	ºC/W

6. Electrical characteristics

(T_C=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	75	-	-	V
Drain-to-source leakage current	I_{DSS}	V_{DS}=75V ,V_{GS}=0V	-	-	1	μA
		T_J=85 ºC	-	-	30	μA
Gate-to-source leakage current	I_{GSS}	V_{GS}=25V,V_{DS}=0V	-	-	100	nA
		V_{GS}=-25V,V_{DS}=0V	-	-	-100	nA
On characteristics						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	3.0	4.0	V
Static drain-source on-resistance[4]	$R_{DS(on)}$	V_{GS}=10V,I_D=75A	-	5.0	6.0	mΩ
Dynamic characteristics[5]						
Input capacitance	C_{iss}	V_{DS}=37.5V,V_{GS}=0V,f=1.0MHz	-	7200	-	pF
Output capacitance	C_{oss}		-	700	-	
Reverse transfer capacitance	C_{rss}		-	460	-	
Gate series resistance	R_G	V_{DS}=0V,V_{GS}=0V,f=1.0MHz	-	1.4	-	Ω
Total gate charge	Q_g	V_{DS}=60V,I_D=75A,V_{GS}=10V	-	145	-	nC
Gate-source charge	Q_{gs}		-	42	-	
Gate-drain (Miller)charge	Q_{gd}		-	54	-	
Resistive switching characteristics[5]						
Turn-on delay time	$T_{d(ON)}$	V_{DD}=37.5V,I_D=75A,V_{GS}=10V, R_G=3.75Ω	-	26	-	nS
Rise time	t_{rise}		-	96	-	
Turn-off delay time	$T_{d(OFF)}$		-	72	-	
Fall time	t_{fall}		-	66	-	
Source-drain body diode characteristics	T_J=25°C,unless otherwise notes					
Diode forward voltage[4]	V_{SD}	V_{GS}=0V,I_S=75A	-	-	1.2	V
Reverse recovery time	t_{rr}	I_{SD}=75A,di_F/dt=100A/μs,	-	42	-	ns
Reverse recovery charge	Q_{rr}		-	64	-	nC

Note: 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

2. Pulse width limited by safe operating area.

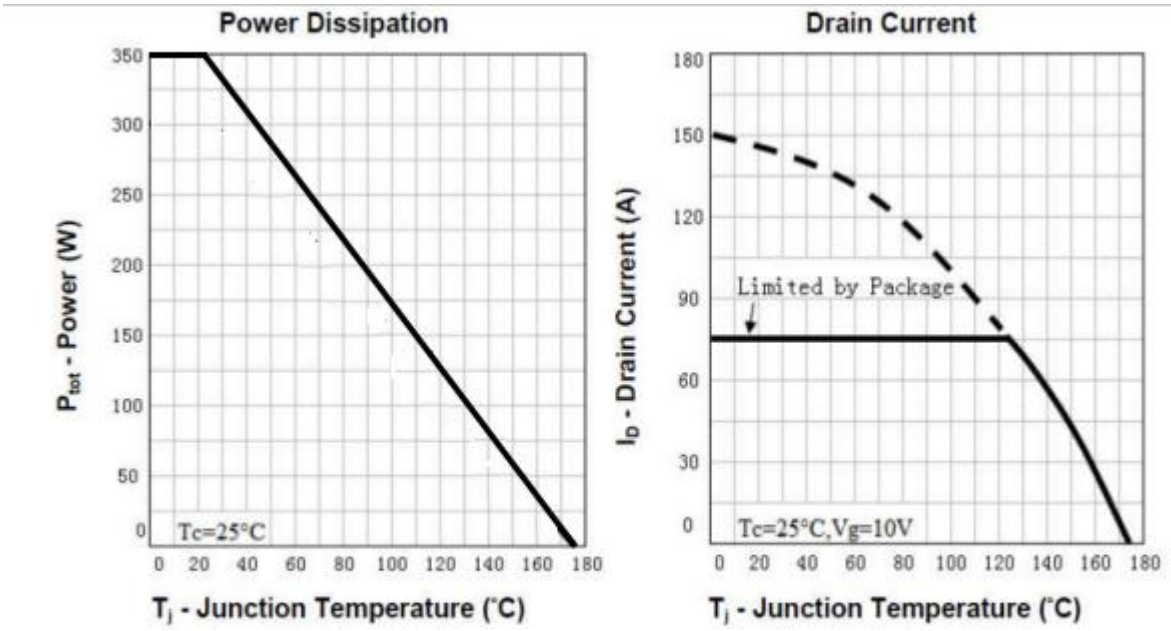
3. Limited by T_{Jmax}, I_{AS}=56A, V_{DD}=48V, R_G=50Ω, Starting T_J=25°C.

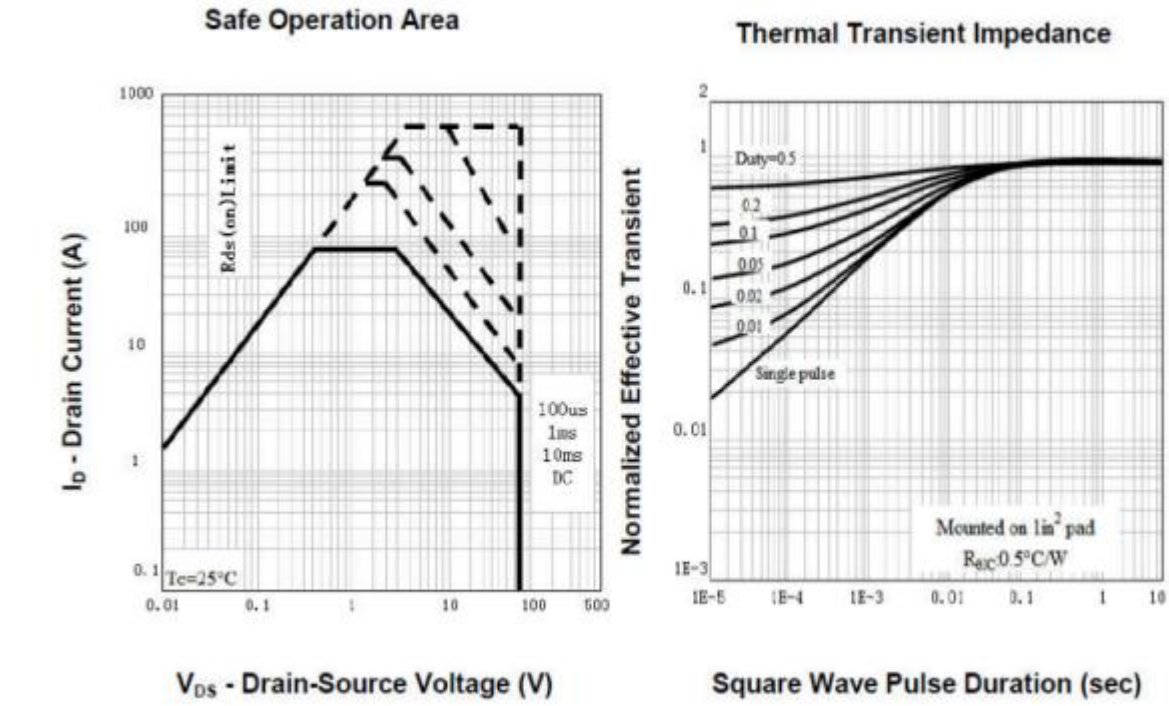
4. Pulse test; Pulse width ≤300μs; duty cycle ≤2%.

5. Guaranteed by design, not subject to production testing.

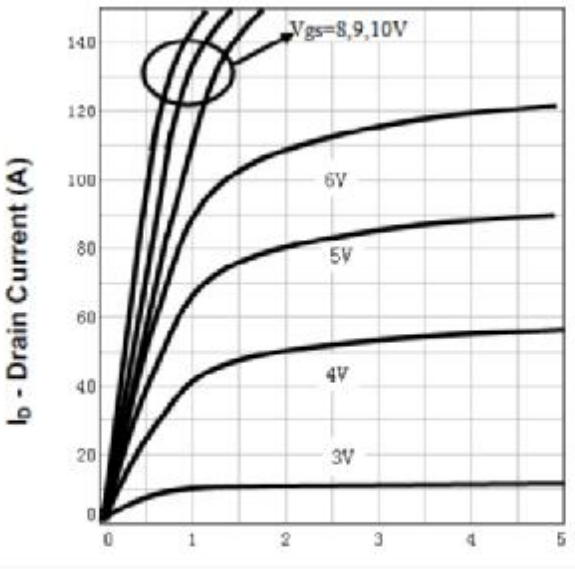
6.KIA finished product specifications please customer before placing order, should obtain the latest version of the finished product specifications.

7. Typical characteristics

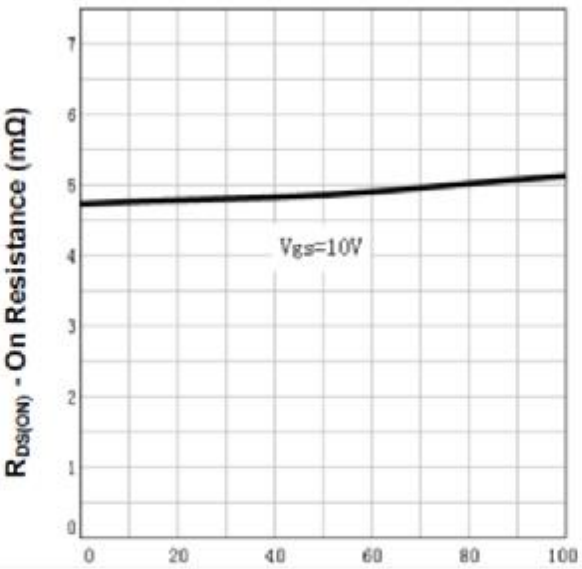




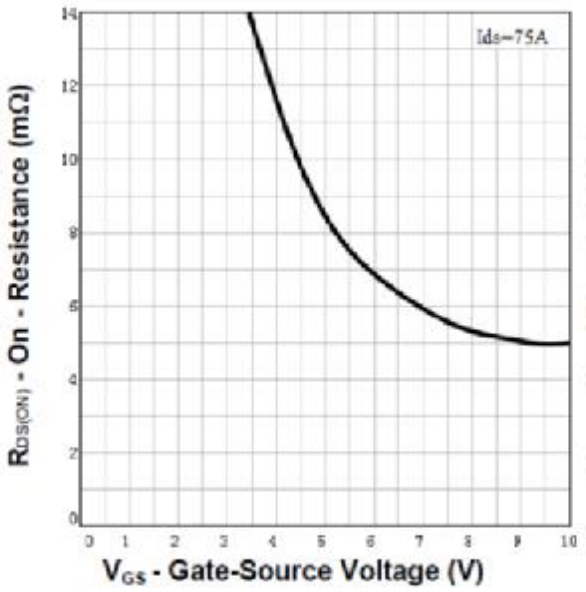
Output Characteristics



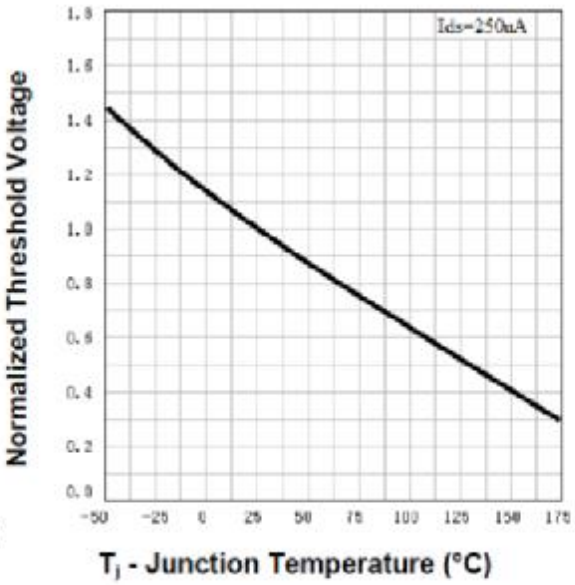
Drain-Source On Resistance



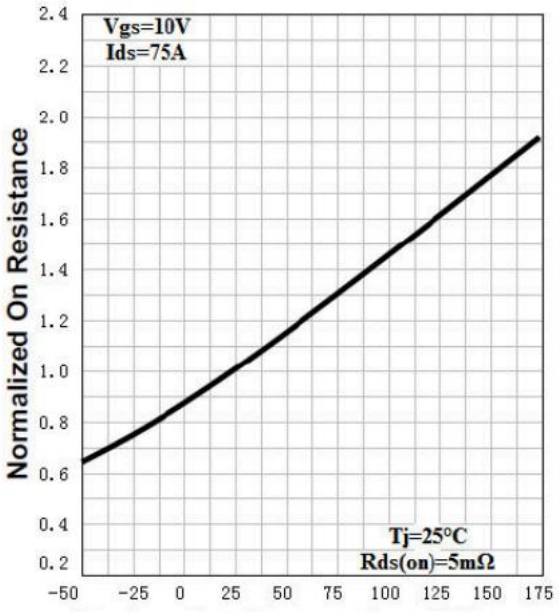
Drain-Source On Resistance



Gate Threshold Voltage

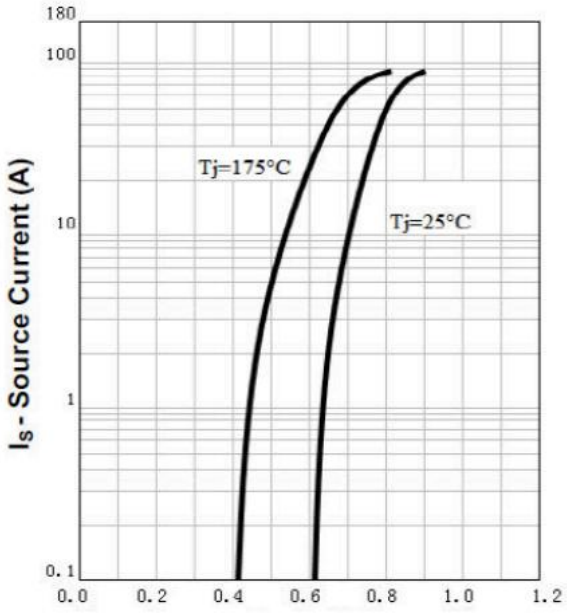


Drain-Source On Resistance



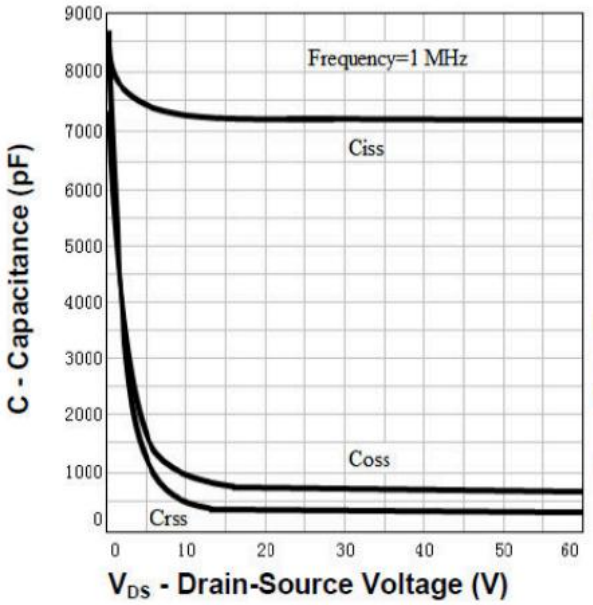
T_j - Junction Temperature (°C)

Source-Drain Diode Forward



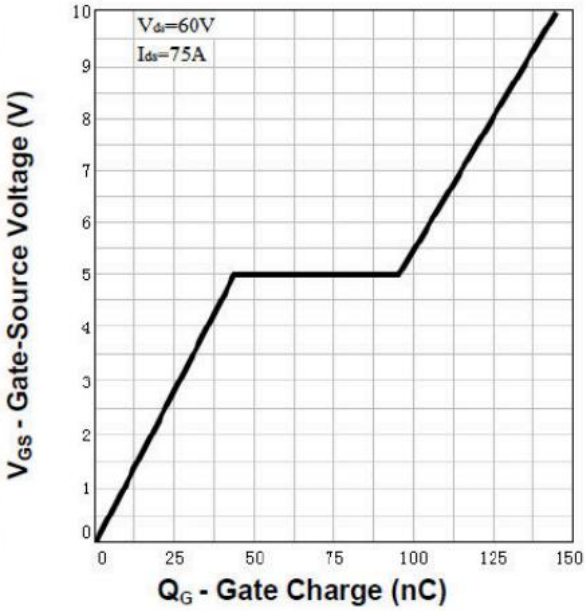
V_{SD} - Source-Drain Voltage (V)

Capacitance



V_{DS} - Drain-Source Voltage (V)

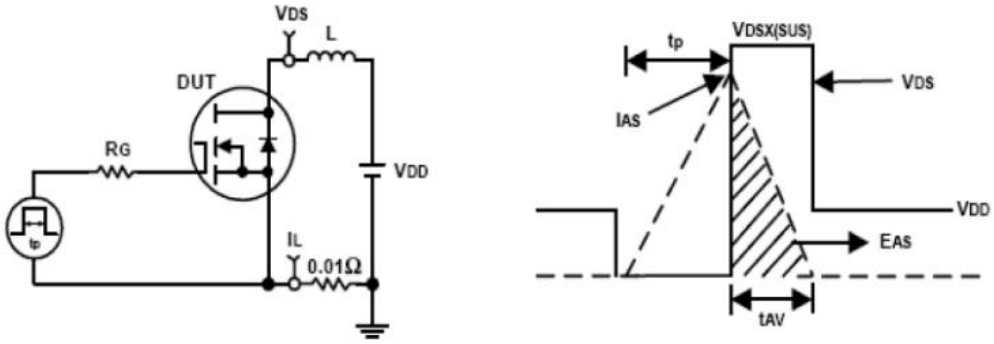
Gate Charge



Q_G - Gate Charge (nC)

8. Test circuits and waveforms

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms